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(54) Radio pager having local- and wide-area reception modes.

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Description

The present invention relates to a radio pager which is capable of operation in a local-area reception mode and in a wide-area reception mode.

Conventional radio pagers are assigned with an identification code representing the user's identification number. The identification code is in the Bose-Chaudhuri-Hocquenghem (31, 16) format for a given local area and transmitted on a specified radio frequency channel. The total number of subscribers available with the BCH (31,16) code format is 65,536. Therefore, if the number of subscribers exceeds the limit, an extra radio frequency channel is required to accommodate new subscribers and this procedure must be repeated in units of 65,625 new subscribers.

A radio pager according to the preamble of Claim 1 is known from WO—A—82/01268 having a multi-scheme signal decoding capability and several communication channels with different decoding schemes. US—A—3,851,251 teaches a BCH coding scheme for several subscribers.

It is an object of the present invention to provide a radio pager which permits efficient utilization of radio frequency channels. This object is solved with the features of Claim 1.

According to the present invention, a pager transmitting station sends paging signals for each called party on first and second channels for local and wide area services, respectively. The paging signal transmitted on the first channel contains an address signal in a first prescribed code format and the paging signal transmitted on the second channel contains an address signal in a second code format, each address signal representing the same identification number assigned to a user of the paging system.

In contrast to the invention the device of WO—A—82/01268 does not realize the advantages of using BCH coding schemes with the same word length but different characteristics for switched local and wide area reception modes.

The present invention will be described in further detail with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a radio pager according to a preferred embodiment of the invention;

Fig. 2 is a block diagram of the decoder of Fig. 1; and

Fig. 3 is a block diagram of a modified embodiment of the invention.

Referring to Fig. 1, there is shown a multi-channel radio paging receiver, or pager according to the present invention. In Fig, 1, first and second paging signals are frequency-modulated respectively upon first and second channels and transmitted from a transmitting station for local and wide area services, respectively. Each paging signal comprises a selective calling address signal and a message signal. The address signal of the first paging signal is in the Bose-Chaudhuri-Hocquenghem (31,16) code format for local area service and the address signal of the second paging signal is in the BCH (31,21) code format for wide area service. The total capacity of codes that can be transmitted on the first channel for local area is 65,536, whereas the total capacity of codes that can be transmitted on the second channel for wide area is 2,097,152, a value 32 times greater than that available for local-area service. This is best understood by analyzing the BCH (31,21) code and BCH (31,16) code as follows. Let it be assumed that generator polynominals are represented by:

$$M_1(x)=x^5+x^2+1$$
$$M_3(x)=x^5+x^4+x3+x^2+1$$
$$M_5(x)=x^5+x^4+x^2+x+1$$

then the generator poloynomial of the BCH (31,21) code is given by:

$$M_1(x) * M_3(x)=x^{10}+x^9+x^8+x^6+x^5+x^3+1$$

and the generator polynomial of the BCH (31,16) code is given by:

$$M_1(x) * M_3(x) * M_5(x)=x^{15}+x^{11}+x^{10}+x^9+x^8+x^7+x^5+x^3+x^2+x+1$$

Since $M_1(x) * M_3(x)$ is a common term of the two generator polynomials, the BCH (31,16) code is a part of the BCH (31,21) code.

The paging signal is intercepted by an antenna 1, filtered through a band-pass amplifier 2 and fed to a frequency converter 3 to which is also applied the output of a variable frequency local oscillator 4. The radio-frequency signal is transported to an intermediate-frequency signal by the frequency converter 3 and fed to a frequency demodulator 5 and thence to a waveshaper 6. Waveshaper 6 comprises a low-pass filter for eliminating undesirable high frequency components of the demodulated signal and a comparator for comparing the output of the low-pass filter with a threshold to generate a digital signal which is a replica of the original signal comprising a message signal preceded by a selective calling signal. The output of waveshaper 6 is connected to a display unit 7 and to a decoder 8 which decodes the address signal by comparing it with an identification code and activates an audio-frequency oscillator 9 to generate an audible tone by a loudspeaker 10 when the address signal coincides with the identification code. Display unit 7 essentially comprises a message decoder and a liquid-crystal display to provide a visual display of a message following an address signal. A user carrying the pager is thus alerted of the reception of a page from a caller.

Variable frequency local oscillator 4 includes a crystal-controlled Colpitts circuit which is formed by a transformer 402 in parallel with a capacitor 403, the transformer being coupled by a parallel circuit of a bypass capacitor 406 and a biasing resistor 407 to the emitter of transistor 408. The emitter of transistor 408

is further coupled to its base by a capacitor 409 and the collector of transistor 408 is connected by a bypass capacitor 411 to ground, by a biasing resistor 410 to its base and directly to a DC voltage source 11. The base of transistor 408 is connected through a local-area selecting circuit to a series of a quartz crystal 414 and a variable capacitor 415 and through a wide-area selecting circuit to a series of a quartz crystal 412 and a variable capacitor 413.

A high-frequency tuning circuit is formed by a transformer 404 and a capacitor 405 connected in parallel therewith. The high-frequency tuning transformer 404 has one end connected through a coupling capacitor 401 to the frequency converter 3. Transformer 402 is connected through an intermediate tap of transformer 404 to ground.

The operating parameters of the local oscillator are determined so that the combined impedance of the two tuning circuits as seen from across the emitter of transistor 408 and ground is capacitive in the variable range of frequencies generated by quartz crystals 412 and 414. In a practical embodiment, each of the quartz crystals has an oscillating frquency which is 1/3 of the difference in frequency between the frequency of the respective channel and the intermediate frequency.

The local-area selecting circuit is established when a first area-selecting switch 12 couples the quartz crystal 414 through contacts 106 and 105 to the base of transistor 408 and the wide-area selecting circuit is established when the switch 12 is moved to a position connecting the quartz crystal 412 through contacts 105 and 104 to the base of the transistor.

Decoder 8 comprises a shift register 80 having 31 bit positions into which the address code is sequentially stored, and a local-area memory 84 and a wide-area memory 83. Local-area memory 84 is enabled by DC voltage source 11 when a second area-selecting switch 13, which is ganged to switch 12, couples the DC source thereto through contacts 102 and 103 and memory 83 is enabled by DC voltage source 11 when the second switch 13 is moved to a position connecting the source voltage thereto through contacts 102 and 101. Each of the memories 83 and 84 has memory cells corresponding in number to the bit positions of shift register 80.

As shown in Fig. 2, each memory cell of memories 83 and 84 is formed by a Zener diode 810, a transistor 820, and a protection resistor 830. Each Zener diode has its cathode connected to an associated input bit line 81 and its anode connected to the base of the associated transistor. Each of the transistors 820 has its collector coupled to a common output line 82 and to contact 101 or 103 through a common resistor 840 and has its emitter connected through the respective resistor 830 to ground.

The user's identification code bits are stored into memory cells by destroying particular Zener diodes to transform them into mere resistance elements. This is accomplished by applying a high positive DC potential to associated input bit lines 81 and a negative DC potential to an output line 82. Resistors 830 serve as a means for protecting the associated transistor from being damaged by the high DC potential. An identification number assigned to the user in the BCH (31,16) code format is stored in local-area memory 84 and the same identification number in the BCH (31,21) code format is stored in a wide-area memory 83.

When a logical "1" input is applied, the memory cell having a destroyed Zener diode develops a logical "0" output at the collector of the associated transistor and the memory cell having a non-destroyed Zener diode develops a logical "1" output, and when a logcial "0" input is applied, the memory cell having a destroyed Zener diode develops a logical "1" output and the cell having a non-destroyed Zener diode develops a logical "0" output. Since the transistors 820 of all cells of each memory are connected in parallel, they establish an AND gate to produce a logical "1" output at the output line 82 when there is a one-to-one coincidence between the address code and identification code. The coincidence output from each memory is coupled by an OR gate 85 to oscillator 9 to activate the speaker 10 and to a control terminal of the display unit 7 to provide a display of a message signal following the address signal.

From the transmitting station, two paging signals respectively having BCH (31,16) and BCH (31,21) formatted address signals are respectively transmitted on the local-area channel and wide-area channel. When the user is in his own local service area, switches 12 and 13 are positioned so that quartz crystal 414 and memory 84 are enabled. Oscillator 4 is tuned to the local-area channel to check the BCH (31,16) address signal transmitted on the local-area channel against the BCH (31,16) identification code stored in memory 84. When the user enters the wide service area, switches 12 and 13 are moved to wide-area service positions so that quartz crystal 412 and memory 83 are enabled. Oscillator 4 is tuned to receive the wide-area channel to decode the BCH (31,21) address signal transmitted on the wide-area channel by comparing it with the BCH (31,21) identification code stored in memory 83.

It is preferred that error correction circuits be provided respectively for correcting errors in the address signals of the BCH (31,21) and BCH (31,16) code formats. In Fig. 3, a 1-bit error correction circuit 86 and a 2-bit error correction circuit 87 are provided to receive the output of waveshaper 6. Each error correction circuit includes a buffer, or shift register into which the received address signal is sequentially loaded in a manner as it is loaded into the shift register of Fig. 2. The address bits stored in the shift register undergo an error correction process known in the art. The 1-bit error correction circuit 86 is connected to the contact 101 so that it is enabled simultaneously with memory 83 during wide-area reception mode and the 2-bit error correction circuit 87 is connected to the contact 103 to be enabled with memory 84 during local-area reception mode. During local-area reception mode, 2-bit error correction is performed by circuit 87 on the address signal of the BCH (31,16) code format and during wide-area reception mode, 1-bit error correction is performed by circuit 86 on the address signal of the BCH (31,21) code format. The error-corrected 31-bit

address signals from error correction circuits 86 and 87 are respectively applied to memories 83 and 84 on input lines 81.

Claims

1. A radio pager comprising

a) a manually controlled selecting means (12,13) for selecting a first channel to operate the pager in a local area reception mode and for selecting a second channel to operate the pager in a wide area reception mode,

b) receiving means (1—6) responsive to said selecting means (12) for receiving a first paging signal which is transmitted on the first channel and for receiving a second paging signal transmitted on the second channel,

c) and decoding means (8) responsive to said selecting means (13) for comparing an address contained in said first paging signal with a user's first identifaction number when said first channel is selected and for comparing an address contained in said second paging signal with a user's second identification number and generating a coincidence signal when the address of said first and second paging signals respectively coincides with said user's first and second identification numbers, characterized in that

d) the address in said first paging signal and the user's first identification number are in a Bose-Chaudhuri-Hocquenghem (BCH (L, M)) code format and the address in said second paging signal and the user's second identification number are in a BCH (L,N) code format, where L>N>M, and that

e) said decoding means (8) comprises:

e_1) a shift register (80) having L-bit positions in which the address of either the received first or second paging signal is sequentially stored; and

e_2) first and second memories (83, 84) respectively operable during said local area reception mode and wide area reception mode, said first and second memories having L-bit memory elements coupled respectively to the L-bit positions of said shift register and memorizing a user's first identification number in said BCH (L,M) code format and user's second identification number in said BCH (L,N) code format, respectively, and for generating a coincidence signal as an indication of reception of said first or second paging signal when the address stored in said shift register coincides with one of said user's identification numbers in said first and second memories.

2. A radio pager as claimed in Claim 1, characterized in that the memory elements of each of said first and second memories comprise a plurality of breakdown diodes (810) and a plurality of transistors (820) forming a plurality of sets with said breakdown diodes, wherein a certain of said breakdown diodes is destroyed in accordance with one of said user's identification numbers, a first electrode of the breakdown diode of each of the sets being connected to a corresponding one of the L-bit positions of the shift register (80), and the transistor of the set having a control electrode connected to a second electrode of the breakdown diode of the set and having controlled electrodes biased to produce an output signal when coincidence occurs between a binary state of the breakdown diode of the set and a binary state of the corresponding bit position of the shift register (80).

3. A radio pager as claimed in Claim 1 or 2, characterized in that said user's first identification number is the same as said user's second identification number.

4. A radio pager as claimed in any one of Claims 1 to 3, characterized in that said decoding means includes a first error correction circuit which is operable during said local area reception mode for providing "i"-bit error correction of the address of said first paging signal, and a second error correction circuit which is operable during said wide area reception mode for providing "j"-bit error correction of the address of said second paging signal, where "j" is smaller than "i".

5. A radio pager as claimed in any one of Claims 1 to 4, characterized in that said integers L, M and N are 31, 16 and 21, respectively.

Patentansprüche

1. Funkrufempfänger mit

a) einer manuell gesteuerten Auswahlrichtung (12, 13) zum Auswählen eines ersten Kanals, um den Rufempfänger in einem Ortsbereichempfangsmodus zu betreiben, und zum Auswählen eines zweiten Kanals, um den Rufempfänger in einem Weitbereichempfangsmodus zu betreiben,

b) Empfangseinrichtungen (1—6), die auf die Auswahleinrichtung (12) ansprechen, um ein erstes Übertragungssignal zu empfangen, das auf dem ersten Kanal gesendet wurde, und zum Empfangen eines zweiten Übertragungssignals, das auf dem zweiten Kanal gesendet wurde,

c) und einer Dekodiereinrichtung (8), die auf die Auswahleinrichtung (13) anspricht, um eine Adresse, die in dem ersten Übertragungssignal enthalten ist, mit einer ersten Kennzahl des Anwenders zu vergleichen, wenn der erste Kanal ausgewählt wird, und um eine Adresse, die im zweiten Übertragungssignal enthalten ist, mit einer zweiten Kennzahl des Anwenders zu vergleichen und ein Koinzidenzsignal zu erzeugen, wenn die Adressen des ersten und zweiten Übertragungssignals mit den ersten und zweiten Kennzahlen des Anwenders übereinstimmen, dadurch gekennzeichnet, daß

d) die Adresse im ersten Übertragungssignal und die erste Kennzahl des Anwenders in einem Bose-

Chaudhuri-Hocquenghem (BCH (,, M))-Codeformat und die Adresse in dem zweiten Übertragungssignal und die zweite Kennzahl das Anwenders in einem BCH (L, N)-Codeformat mit L>N>M sind, und daß

e) die Dekodiereinrichtung (8) aufweist:

e_1) ein Schieberegister (80) mit L-Bit-Positionen, in denen die Adresse eines der empfangenen ersten oder zweiten Übertragungssignale aufeinanderfolgend gespeichert wird; und

e_2) erste und zweite Speicher (83, 84), die während des Ortsbereich- und des Weitbereichempfangsmodus betrieben werden können, wobei die ersten und zweiten Speicher L-Bit-Speicherelemente aufweisen, die an die L-Bit-Positionen des Schieberegisters gekoppelt sind und eine erste Kennzahl eines Anwenders in dem BCH (L, M)-Codeformat und eine zweite Kennzahl des Anwenders in dem BCH (L, N)-Codeformat speichert, und zum Erzeugen eines Koinzidenzsignals als eine Darslellung des Empfangs des ersten oder zweiten Übertragungssignals, wenn die im Schieberegister gespeicherte Adresse mit einer der Kennzahlen des Anwenders in den ersten und zweiten Speichern übereinstimmt.

2. Funkrufempfänger nach Anspruch 1, dadurch gekennzeichnet, daß die Speicherelemente jedes der ersten und zweiten Speicher mehrere Durchbruchsdioden (810) und mehrere Transistoren (820) aufweisen, die mit den Durchbruchsdioden mehrere Gruppen ausbilden, wobei eine bestimmte der Durchbruchsdioden in Übereinstimmung mit einer der Kennzahlen des Anwenders zerstört wird, eine erste Elektrode der Durchbruchsdiode jeder der Gruppen mit einer entsprechenden der L-Bit-Positionen des Schieberegisters (80) verbunden wird, und der Transistor der Gruppe eine Steuerelektrode aufweist, die mit einer zweiten Elektrode der Durchbruchsdiode der Gruppe verbunden ist und gesteuerte Elektroden aufweist, die vorgespannt sind, um ein Ausgangssignal zu erzeugen, wenn zwischen einem binären Zustand der Durchbruchsdiode der Gruppe und einem binären Zustand der entsprechenden Bit-Position des Schieberegisters (80) Koinzidenz auftritt.

3. Funkrufempfänger nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die erste Kennzahl des Anwenders gleich der zweiten Kennzahl des Anwenders ist.

4. Funkrufempfänger nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, daß die Dekodiereinrichtung einen ersten Fehlerkorrekturschaltkreis aufweist, der während des Ortsbereichempfangsmodus betrieben werden kann, um eine "i"-Bit-Fehlerkorrektur der Adresse des ersten Übertragungssignals zu liefern, und einen zweiten Fehlerkorrekturschaltkreis aufweist, der während des Weitbereichempfangsmodus betrieben werden kann, um eine "j"-Bit-Fehlerkorrektur der Adresse des zweiten Übertragungssignals zu liefern, wobei "j" kleiner als "i" ist.

5. Funkrumpfempfänger nach einem der Ansprüche 1 bis 4, dadurch gekennzeichnet, daß die ganzen Zahlen L, M und N 31, 16 bzw. 21 sind.

Revendications

1. Dispositif radio de recherche de personnes, comprenant:

a) un moyen (12, 13) de sélection commandé manuellement pour choisir un premier canal de manière à faire fonctionner le dispositif dans un mode de réception en zone locale et à sélectionner un second canal pour faire fonctionner le dispositif dans un mode de réception en zone étendue,

b) un moyen de réception (1—6) répondant au moyen de sélection (12) pour recevoir un premier signal de recherche de personnes qui est transmis sur le premier canal et pour recevoir un second signal de recherche de personnes qui est transmis sur le second canal,

c) et un moyen de décodage (8) répondant au moyen de sélection (13) pour comparer une adresse contenue dans le premier signal de recherche de personnes à un premier numéro d'identification d'utilisateur lorsque le premier canal est choisi et pour comparer une adresse contenue dans le second signal de recherche de personnes à un second numéro d'identification de l'utilisateur et produire un signal de coïncidence lorsque les adresses des premier et second signaux de recherche de personnes respectivement coïncident avec les premier et second numéros d'identification de l'utilisateur, caractérisé en ce que:

d) l'adresse dans le premier signal de recherche de personnes et le premier numéro d'identification de l'utilisateur sont dans un format de code Bose-Chaudhuri-Hocquenghem (BCH (L,M)) et l'adresse du second signal de recherche de personnes et le second numéro d'identification de l'utilisateur sont dans un format du code BCH (L, N), où L>N>M, et en ce que:

e) le moyen de décodage (8) comprend:

e_1) un registre à décalage (80) ayant des positions de L-bits dans lesquelles l'adresse soit du premier soit du second signal reçu de recherche de personnes est séquentiellement stockée; et

e_2) des première et seconde mémoire (83, 84) pouvant être respectivement mises en oeuvre pendant le mode de réception en zone locale et le mode de réception en zone étendue, les première et seconde mémoires ayant des éléments de mémoire de L-bits couplés respectivement aux positions de L-bits zu registre à décalage et mémorisant un premier numéro d'identification de l'utilisateur dans le format du code BCH (L, M) et le second numéro d'identification de l'utilisateur dans le format du code BCH (L, N), respectivement, et générant un signal de coïncidence comme une indication de la réception des premier ou second signaux de recherche de personnes lorsque l'adresse stockée dans le registre à décalage coïncide avec l'un des numéros d'identification de l'utilisateur dans les première et seconde mémoires.

2. Dispositif radio de recherche de personnes selon la revendication 1, caractérisé en ce que les

éléments de mémoire de chacune des première et seconde mémoires comprennent une multitude de diodes à seuil d'amorçage (810) et une multitude de transistors (820) formant une multitude de jeux avec les diodes à seuil d'amorçage, où une certaine diode parmi les diodes à seuil d'amorçage est détruite en conformité avec l'une des numéros d'identification de l'utilisateur, une première électrode de la diode à seuil d'amorçage de chacun des jeux étant connectée à une position correspondante des positions des L-bits du registre à décalage (80), et le transistor du jeu ayant une électrode de commande connectée à une seconde électrode de la diode à seuil d'amorçage du jeu et ayant des électrodes commandées qui sont polarisées de manière à produire un signal de sortie lorsqu'il se produit une coïncidence entre un état binaire de la diode à seuil d'amorçage du jeu et un état binaire de la position correspondante du bit du registre à décalage (80).

3. Dispositif radio de recherche de personnes selon la revendication 1 ou 2, caractérisé en ce que le premier numéro d'identification de l'utilisateur est le même que le second numéro d'identification de l'utilisateur.

4. Dispositif radio de recherche de personnes selon l'une quelconque des revendications 1 à 3, caractérisé en ce que le moyen de décodage comporte un premier circuit de correction d'erreur qui peut fonctionner pendant le mode de réception en zone locale pour fournir une correction d'erreur du bit "i" de l'adresse du premier signal de recherche de personnes, et un second circuit de correction d'erreur qui peut fonctionner pendant le mode de réception en zone étendue pour fournir une correction d'erreur du bit "j" de l'adresse du second signal de recherche de personnes, où "j" est inférieur à "i".

5. Dispositif radio de recherche de personnes selon l'une quelconque des revendications 1 à 4, caractérisé en ce que les nombres entiers L, M et N sont 31, 16 et 21, respectivement.

FIG. 1

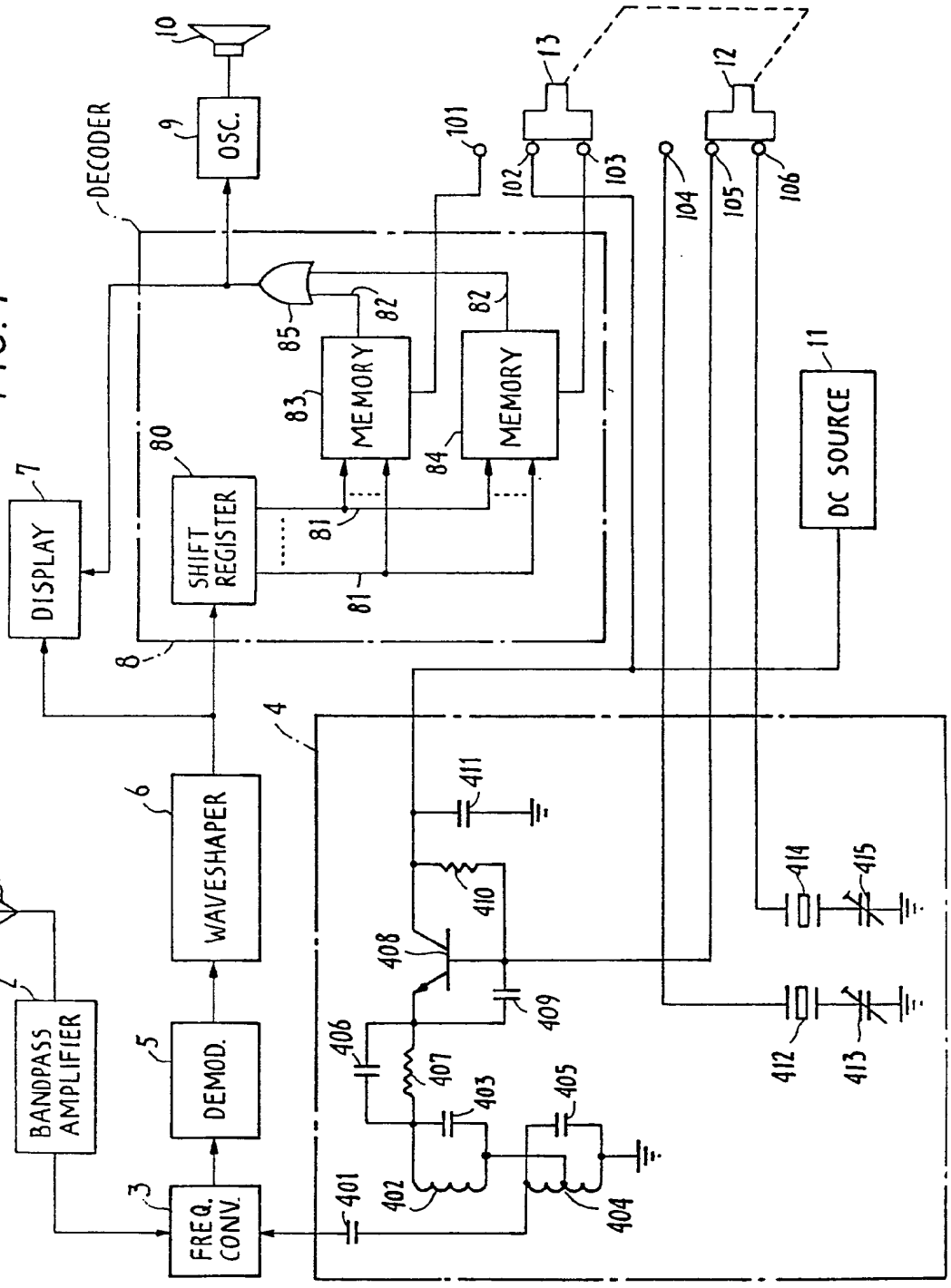
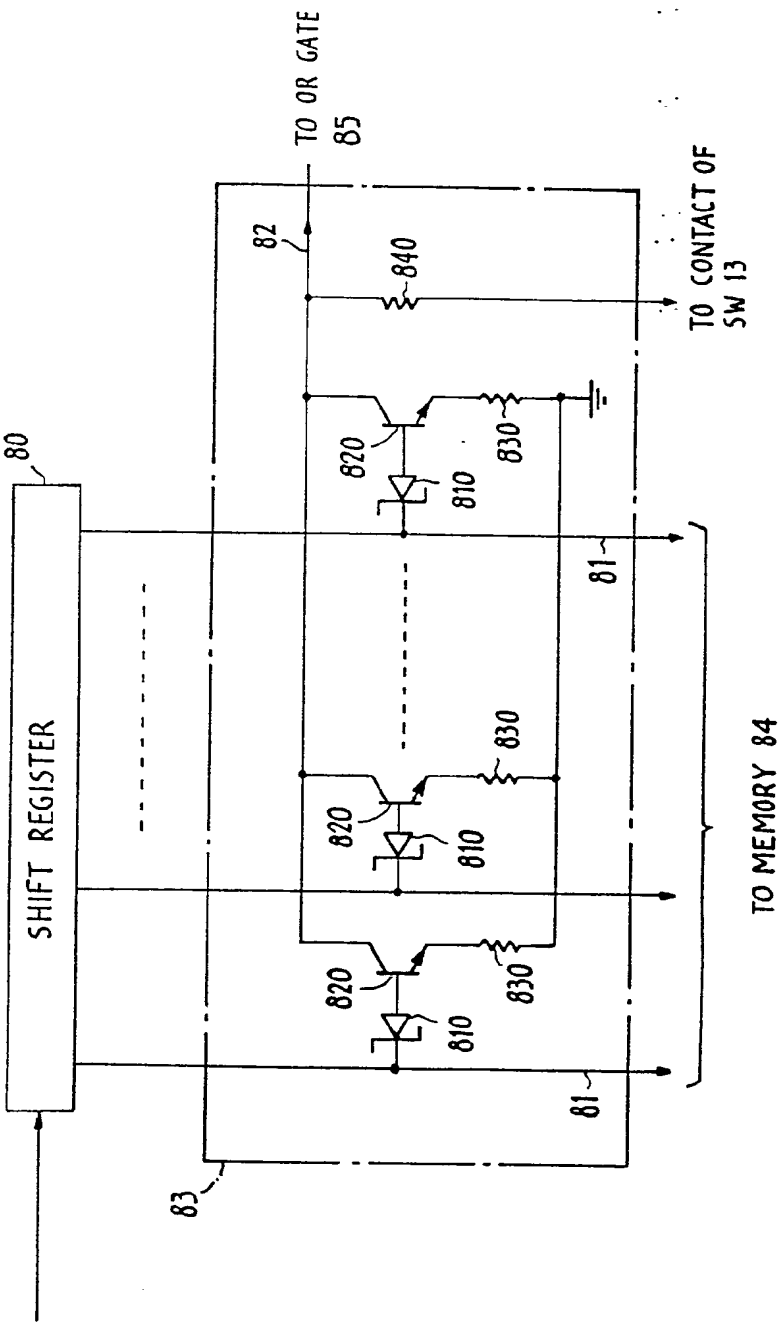

1
2
BANDPASS AMPLIFIER
3
FREQ. CONV.
4
5
DEMOD.
6
WAVESHAPER
7
DISPLAY
8
DECODER
9
OSC.
10
11
DC SOURCE
12
13
80
SHIFT REGISTER
81
82
83
MEMORY
84
MEMORY
85
101
102
103
104
105
106
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415

FIG. 2


TO OR GATE
85
82
840
TO CONTACT OF
SW 13
80
SHIFT REGISTER
820
810
830
81
TO MEMORY 84
83

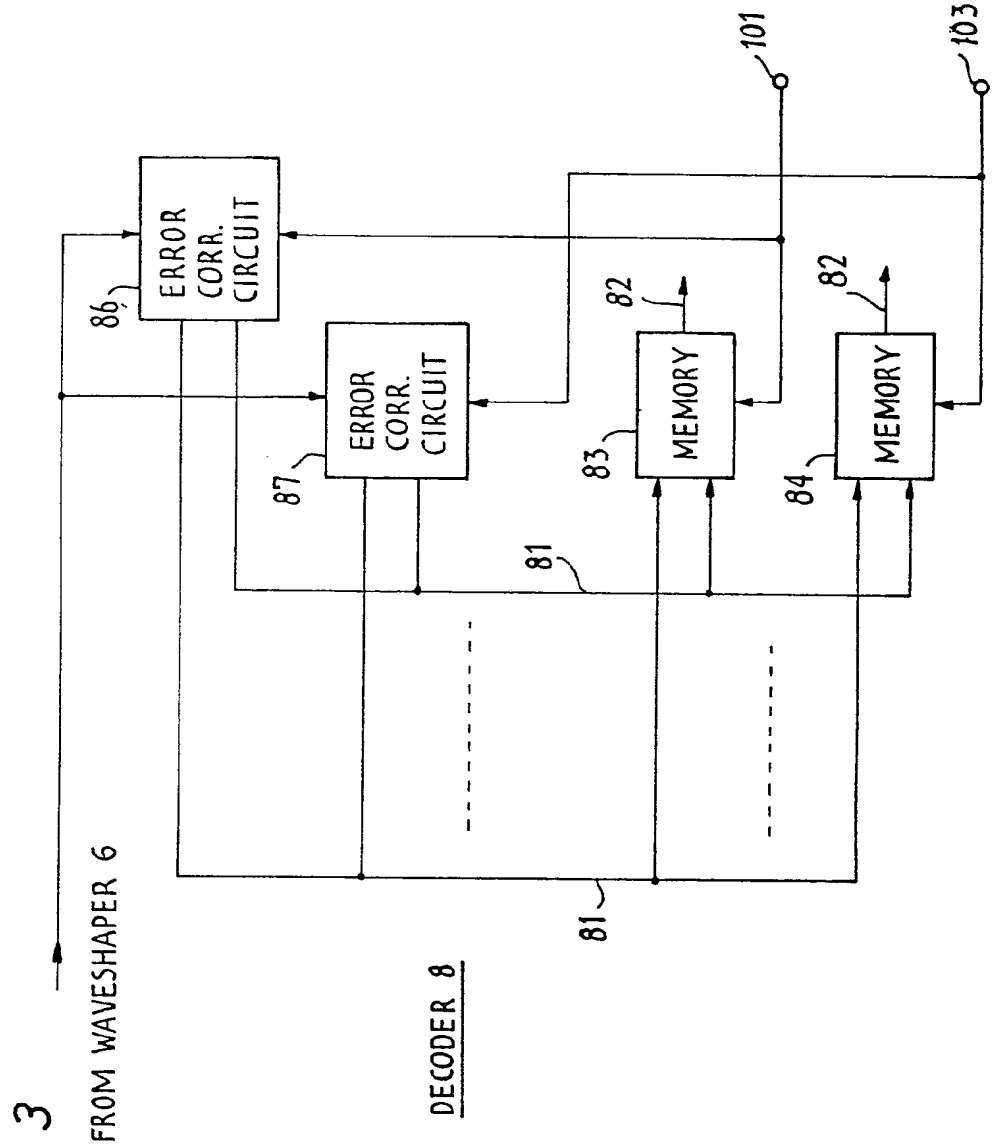

FROM WAVESHAPER 6
DECODER 8
ERROR CORR. CIRCUIT
ERROR CORR. CIRCUIT
MEMORY
MEMORY
86
87
82
83
82
84
81
81
101
103

FIG. 3